# UG 3rd Semester Examination 2021

## PHYSICS (Honours)

## Paper : DC - 7

[CBCS]

Full Marks : 25 Time : Two Hours

*The figures in the margin indicate full marks. Candidates are required to give their answers in their own words as far as practicable.*

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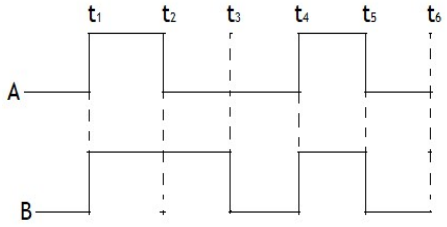
1. Answer any ***five*** of the following questions. 5×2=10

   (a) Why is an exclusive-NOR gate called an equality detector?

   (b) Show that $\overline{\bar{A}B + A\bar{B}} = AB + \bar{A}\bar{B}$.

   (c) Two waveforms are applied to a 2-input NAND gate as shown in figure below. Sketch the output wave form.




   (d) Simplify the Boolean expression $Y = \bar{A}B + AB\bar{C} + ABC$ using a Karnaugh map.

   (e) Distinguish between combinational and sequential logic circuits.

   (f) Define the term 'decoder'. Show how to decode the 4-bit code 1011(LSB).

   (g) Use both 1's and 2's complement method separately to perform the following binary subtractions:

   11011 - 01101

   (h) Convert hexadecimal number 3A9E.B0D to a binary one.

2. Answer any ***three*** of the following questions. 3×5=15

(a) (i) Show that $(A \oplus B) \oplus C = A \oplus (B \oplus C)$

(ii) Using Karnaugh map minimize the following logic expression:

$Y = ABCD + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + \bar{A}B\bar{C}D + \bar{A}\bar{B}CD + AB\bar{C}\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D}$ 2+3=5

(b) What is edge triggering in a flip-flop? Draw the circuit diagram of a 4bit register using J-K flip flops. Write down a table for readings of the shift register after each clock pulse by assuming the data word 1011. 1+2+2=5

(c) Draw the logic diagram of a four-bit synchronous binary down counter using:

(I) JK flip-flops that trigger on the positive-edge of the clock.

(II) T flip-flops that trigger on the negative edge of the clock. $2\frac{1}{2} + 2\frac{1}{2} = 5$

(d) What is read only memory? Show that a ROM may be considered as a decoder for the input code followed by an encoder for the output code. 2+3=5

(e) What is the difference between a half adder and a full adder? Give the truth table of a full adder and hence show that a full adder can be constructed using two half adders and an OR gate.

2+3=5

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